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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO	
10/086,655	(02/28/2002	E. Henry Stevens	291958174US01	8295	
25096	7590	02/02/2004	•	EXAMINER		
PERKINS (COIE LL	P		BERRY, F	LENEE R	
PATENT-SE P.O. BOX 12				ART UNIT	PAPER NUMBER	
SEATTLE, WA 98111-1247				2818		

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary - The MAILING DATE of this communication appears on the cover shoot with the correspondence address - Period for Repty A SHORTENEO STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time map be available under the purptions of 27 CR 1.736(a). In ne event, however, may a reply be timely filed Extensions of time map be available under the purptions of 27 CR 1.736(a). In ne event, however, may a reply be timely filed Extensions of time map be available under the purptions of 27 CR 1.736(a) in ne event, however, may a reply be timely filed Extensions of timely specified above is less than their) (001 days, a reply within the abattery minimum of thirty (30) days will be considered timely. If the period for reply reported legislate power is the period filed on the period (and the period of the period		Application No.	Applicant(s)				
Renee R Berry 2818	Office Action Commons	10/086,655	STEVENS, E. HENRY				
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2a) This action is FINAL. 2b) This action is non-final. 3 Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11(453 O.G. 213. Disposition of Claims 4) Claim(s) 52-69 is/are pending in the application. 4a) Of the above claim(s) 52-56 is/are withdrawn from consideration. 5 Claim(s) 57-69 is/are allowed. 6 Claim(s) 57-69 is/are rejected. 7 Claim(s) is/are objected to. 8 Claim(s) is/are objected to. 8 Claim(s) is/are subject to restriction and/or election requirement. Application Papers 9 The specification is objected to by the Examiner. 10 The drawing(s) filed on 28 February 2002 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11 The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. §§ 119 and 120 12 Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * ○ None of:	THE MAILING DATE OF THIS COMMUNICAT - Extensions of time may be available under the provisions of 37 after SIX (6) MONTHS from the mailing date of this communice - If the period for reply specified above is less than thirty (30) day - If NO period for reply is specified above, the maximum statutory - Failure to reply within the set or extended period for reply will, but any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).	FION. CFR 1.136(a). In no event, however, may a ration. s, a reply within the statutory minimum of thir y period will apply and will expire SIX (6) MON by statute, cause the application to become AB	eply be timely filed by (30) days will be considered timely. THS from the mailing date of this communication. DANDONED (35 U.S.C. § 133).				
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DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Group II is acknowledged.

Claims 52-56 are withdrawn from further consideration pursuant to 37 CFR

1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 57-69 are rejected under 35 U.S.C. 102(e) as being anticipated by US patent no. 6,420,262 to Farrar.

In regards to claim 57, Farrar teaches a method of fabricating interconnect metallization structures on a workpiece, comprising: applying a conductive barrier layer to the workpiece in a film deposition tool set; forming a patterned resist layer on the workpiece, the patterned resist layer being a mask having openings in a pattern of interconnect metallization structure plating a metal into the openings of the resist layer in a wet processing tool set to form the interconnect metallization structures; and altering portions of the barrier layer to electrically isolate the interconnect metallization

Application/Control Number: 10/086,655

Art Unit: 2818

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structures from each other in the wet processing tool set at column 7, lines 19-32 and column 8, lines 55-62.

In regards to claim 58, teaches plating a metal into the openings comprises electroplating copper onto exposed portions of the barrier layer in the openings.

In regards to claim 59, teaches applying a seed layer onto the barrier layer in the film deposition tool set, and wherein (a) the openings in the resist layer expose portions of the seed layer and (b) plating a metal into the openings comprises electroplating copper onto the exposed portions of the seed layer.

In regards to claim 60, teaches a protective layer onto surfaces of the interconnect metallization electroplating structures.

In regards to claim 61, Farrar teaches altering portions of the barrier layer to electrically isolate the interconnect metallization structures from each other comprises oxidizing portion: of the barrier layer between the interconnect structures at column 8, lines 42-46.

In regards to claim 62, Farrar teaches altering portions of the barrier layer to electrically isolate the interconnect metallization structures from each other comprises removing portions of the barrier layer between the interconnect structures at column 11, lines 20-26.

In regards to claim 63, Farrar teaches applying a seed layer onto the barrier layer in the film deposition tool set and wherein altering portions of the barrier layer to electrically isolate the interconnect metallization structures from each other comprises

Art Unit: 2818

oxidizing portions of the barrier layer between the interconnect structures at column 10, lines 60-67.

In regards to claim 64, Farrar teaches applying a seed layer onto the barrier layer in the film deposition tool set, and wherein altering portions of the barrier layer to electrically isolate the interconnect metalllization structures from each other comprises removing portions of the barrier layer between the interconnect structures at column 10, lines 60-65.

In regards to claim 65, Farrar teaches a method of making metal interconnect structures on a workpiece, comprising applying a barrier layer to the workpiece in a first deposition station of a film deposition tool set; applying a copper seed layer to the barrier layer in a second deposition station of the film tool set, forming a patterned mask of a resist on the copper seed layer, the patterned mask having a plurality of openings defining locations form forming raised metal interconnect structures on the seed layer; plating copper onto the copper seed layer in the openings of the patterned mask in a first wet processing station of a wet tool set to form copper interconnect structure; removing the patterned mask in second wet processing station of the wet tool set; and removing portions of the seed layer between the copper interconnect structures in a third wet processing station of the wet tool set at column 9, lines 31-48, Figure 2C.

In regards to claim 66, Farrar teaches plating copper onto the copper seed layer comprises electroplating copper at column 11, lines 36-39.

In regards to claim 67, Farrar teaches plating copper onto the copper seed layer comprises electroplating copper; and removing portions of the seed layer between the

Application/Control Number: 10/086,655

Art Unit: 2818

copper interconnect structures comprises etching the copper seed layer at column 11,

lines 30-39.

In regards to claim 68, Farrar teaches plating copper onto the copper seed layer

Page 5

comprises electroplating copper; and the method further comprises exposing the

workpiece to an oxygen-containing environment to form a first oxide on the copper

interconnect structures, removing the first oxide over the copper interconnect structures,

and plating a protective layer onto surfaces of the copper Interconnect structures at

column 11, lines 10-39.

In regard to claim 69, Farrar teaches removing portions of the seed layer

between the copper interconnect structures comprises removing the second oxide from

between the copper interconnect structures at column 11, lines 20-27.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R Berry whose telephone number is (571) 272-

1174. The examiner can normally be reached on M-F 9-5:30.

RRR

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